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Appl. No. 10/709,652 Amdt. Dated 01/04/2006 Reply to Office action of November 29, 2005 Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

## Listing of Claims:

Claims 1-9 were previously canceled.

Cancel claims 10, 15, 16, 18.

Amend the remaining claims, as follows.

10. (canceled) A method of forming a spacer for a gate electrode of a transister comprising the steps:

depositing a dielectric material; etching the dielectric material to form a spacer; forming porces in the dielectric material; and depositing a thin layer over the percus dielectric material.

11. (previously presented) A method of forming a spacer for a gate electrode of a transistor comprising the steps:

depositing a dielectric material;

etching the dielectric material to form a spacer;

forming pores in the dielectric material; and

depositing a thin layer over the porous dielectric material;

wherein:

the spacer is made porous by exposing the spacers to an oxygen plasma.

12. (previously presented) A method of forming a spacer for a gate electrode of a transistor comprising the steps:

depositing a dielectric material;

etching the dielectric material to form a spacer;

forming pores in the dielectric material; and

depositing a thin layer over the porous dielectric material;

wherein:

the spacer comprises organic material; and

the spacer is made porous by removing the organic material.

13. (currently amended) The method, according to claim 10 12, wherein: the spacer comprises a Si-O-C-N type of low-k material.

14. (previously presented) A method of forming a spacer for a gate electrode of a transistor comprising the steps:

depositing a dielectric material;

etching the dielectric material to form a spacer;

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forming pores in the dielectric material; and
depositing a thin layer over the porous dielectric material;
wherein:

the pores are formed during the spacer etch, rather than during deposition of the dielectric material.

- 15. (canceled) The method, according to claim 10, wherein the spacer has a reduced dielectric constant (k).
- 16. (canceled) The method, assording to claim 15, wherein the reduced dielectric constant (k) is less than 3.85.
- 17. (previously presented) A method of forming a spacer for a gate electrode of a transistor comprising the steps:

depositing a dielectric material; etching the dielectric material to form a spacer; forming pores in the dielectric material; and depositing a thin layer over the porous dielectric material; wherein the spacer has a reduced dielectric constant (k); wherein the reduced dielectric constant (k) is less than 7.0, but greater than 3.85.

- 18. (canceled) The method, according to claim 15, wherein the spacer is peroue, and further comprising depositing a thin layer on the spacer to prevent moisture aborption.
- 19. (currently amended) The method, according to claim 10 11, wherein the thin layer comprises oxide.
- 20. (currently amended) The method, according to claim 10 11, wherein the thin layer has a thickness of less than 5nm.
- 21. (previously presented) The method, according to claim 11, wherein: the spacer comprises a Si-O-C-N type of low-k material.
- 22. (previously presented) The method, according to claim 14, wherein: the spacer comprises a Si-O-C-N type of low-k material.
- 23. (previously presented) The method, according to claim 17, wherein: the spacer comprises a Si-O-C-N type of low-k material.
- 24. (previously presented) The method, according to claim 11, wherein: the spacer has a reduced dielectric constant (k); and the reduced dielectric constant (k) is less than 3.85.
- 25. (previously presented) The method, according to claim 14, wherein:

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the spacer has a reduced dielectric constant (k); and the reduced dielectric constant (k) is less than 3.85.

- 26. (currently amended) The method, according to claim 17 12, wherein: the spacer has a reduced dielectric constant (k); and the reduced dielectric constant (k) is less than 3.85.
- 27. (previously presented) The method, according to claim 11, wherein the thin layer comprises a material selected from the group consisting of oxide, amorphous silicon and nitride.
- 28. (previously presented) The method, according to claim 14, wherein the thin layer comprises a material selected from the group consisting of oxide, amorphous silicon and nitride.
- 29. (previously presented) The method, according to claim 17, wherein the thin layer comprises a material selected from the group consisting of oxide, amorphous silicon and nitride.

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- -- 30. (new) The method, according to claim 12, wherein the thin layer comprises a material selected from the group consisting of oxide, amorphous silicon and nitride. --
- -- 31. (new) The method, according to claim 12, wherein the thin layer has a thickness of less than 5nm. --
- 32. (new) The method, according to claim 17, wherein the thin layer comprises a material scleeted from the group consisting of oxide, amorphous silicon and nitride. --
- -- 33. (new) The method, according to claim 14, wherein the thin layer has a thickness of less than 5nm. --